REPLY BRIEF TRANSMITTAL LETTER

June 21, 2005

MAIL STOP APPEAL BRIEF - PATENTS
COMMISSIONER FOR PATENTS
P.O. Box 1450
ALEXANDRIA, VA 22313-1450

Re: Appellants: Carns et al.
Assignee: ZiLOG, Inc.
Title: "Process to Improve High Performance Capacitor Properties in Integrated MOS Technologies"
Serial No.: 09/351,544 Filed: July 12, 1999
Examiner: N. Drew Richards Art Unit: 2815
Atty. Docket No.: ZIL-204

Dear Sir:

Transmitted herewith are the following documents:
(1) Request That Appeal Be Maintained and a Reply Brief (33 pages);
(2) a copy of a non-patent document relied upon by the Examiner;
(3) Return Postcard; and
(4) This transmittal sheet.

☒ No additional Fee is required.
☐ The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	27*	minus	61	0	$50	$0.00
INDEP. CLAIMS	3	minus	12	0	$200	$0.00
Total Additional Claim Fee						$0.00
Fee for Appeal Brief [§41.20(b)(2)]**						$0.00
Fee for Request for Oral Hearing [§41.20(b)(3)]**						$0.00
Fee for Extension of Time (__ month)						$0.00
* includes 6 withdrawn claims					TOTAL	$0.00
** previously paid						$0.00

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By Darien K. Wallace
Darien K. Wallace

Date of Deposit: June 21, 2005

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Carns et al.

Assignee: ZiLOG, Inc.

Title: "Process to Improve High Performance Capacitor Properties in Integrated MOS Technologies"

Appl. No.: 09/351,544 Filing Date: July 12, 1999

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Mail Stop Appeal Brief - Patents
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P.O. Box 1450
Alexandria, VA 22313-1450

June 21, 2005

REPLY BRIEF AND REQUEST THAT APPEAL BE MAINTAINED

Appellants hereby request, pursuant to 37 CFR § 41.39(b)(2), that the appeal first noticed on April 20, 2004, be maintained. This Request That Appeal Be Maintained is accompanied by this Reply Brief pursuant to 37 CFR § 41.37(c). This Reply Brief supersedes the Supplemental Appeal Brief filed on October 18, 2004. A request for an oral hearing was submitted together with the Supplemental Appeal Brief.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, ZiLOG, Inc., as named in the caption above.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals and Interferences (the "Board") in the pending appeal.

III. STATUS OF CLAIMS

The application at issue, filed on July 12, 1999, included 30 claims. In various amendments, claims 31-114 were added, and claims 1-2, 12-35, 40-71 and 75-101 were cancelled. In a final office action dated January 20, 2004, the Examiner withdrew claims 109-114 due to the claims being drawn to a constructively elected invention. Appellants reserved the right to pursue claims 109-114 at a later time.

The office action dated January 20, 2004, was responsive to an amendment dated November 3, 2003 (referred to in the office action as a communication filed on "06 November 2003"). The office action dated January 20, 2004, finally rejected claims 3-11, 36-39, 72-74, 102-108. Appellants responded with a response dated March 16, 2004, in which no claims were added, amended or cancelled. An advisory action dated March 31, 2004, stated that claims 3-11, 39, 72-74, 102-108 were rejected, and claims 109-114 were withdrawn. The advisory action dated March 31, 2004, did not mention claims 36 and 37. Appellants filed a first appeal brief on June 21, 2004, which was accompanied by an amendment in which Appellants cancelled claims 107-108. Thus, claims 3-11, 36-39, 72-74 and 102-106 were the subject of the first appeal.

The Examiner did not submit an answer to the first appeal brief dated June 21, 2004, but rather reopened prosecution and entered an Office Action dated August 12, 2004 (the "Office Action"). The Office Action is not responsive to the arguments of Appellants in the first appeal brief. The Office Action states that it is responsive to the amendment dated November 3, 2003 (referred to in the Office Action as a communication filed on "06 November 2003"). In the Office Action, claims 3-11, 36-39, 72-74, 102-108 stand finally rejected. Considering that Appellants cancelled claims 107-108 in the amendment that accompanied Appellants' first appeal brief dated June 21, 2004, claims 3-11, 36-39, 72-74, 102-106 are the subject of this Appeal.

IV. STATUS OF AMENDMENTS

Of the claims 3-11, 36-39, 72-74, 102-106 that are the subject of this Appeal, Appellants added claims 102-106 in the amendment dated November 3, 2003. In the amendment dated November 3, 2003, no other changes were made to the claims that are the subject of this Appeal, and no amendments were made to the drawings or to the specification.

No amendments were made in the response dated March 16, 2004 that was filed subsequent to the final office action dated January 20, 2004. In the amendment that accompanied Appellants' first appeal brief dated June 21, 2004, claims 107-108 were cancelled, but no other changes were made. Therefore, the statement at paragraph 12 of the Office Action, "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action" is inaccurate. No amendment accompanies this Reply Brief. The listing of claims in the Claims Appendix (section X below) is identical to the listing of claims submitted with Appellants' first appeal brief dated June 21, 2004.

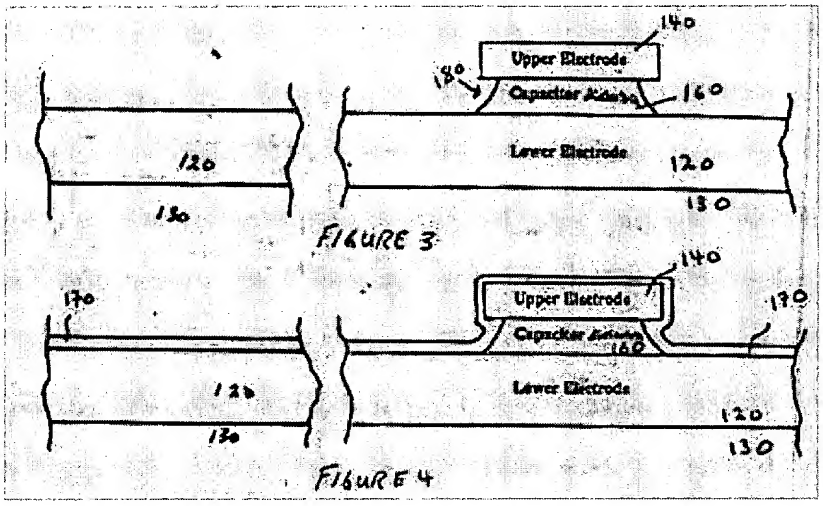
The Examiner did not submit an answer to the first appeal brief, but rather reopened prosecution and entered the Office Action, which cited multiple prior art references for the first time. The new ground of rejection in the Office Action was made final, even though it was neither (A) necessitated by an amendment by Appellants (as no such amendment was made), nor (B) based on information presented in an information disclosure statement. See MPEP § 1208.02 Reopening of Prosecution After Appeal (most-current version August 2001).

V. SUMMARY OF CLAIMED SUBJECT MATTER[1]

A capacitor is formed in an integrated circuit by forming a lower electrode layer 120 on a semiconductor body 130, as shown in figures 3 and 4 of the above-captioned patent application. (See figures 3 and 4 below.) A dielectric

[1] The following summary pursuant to 37 CFR §41.37(c)(1)(v) is a concise explanation of the claims and is to be read in light of the disclosure. This summary does not limit the claims. (See MPEP §1206)

layer 160 is formed over a portion of the lower electrode layer 120, and an upper electrode layer is formed over a portion of the dielectric layer 160. A portion of the upper electrode layer is removed to expose a portion of the dielectric layer, thereby forming an upper electrode 140 of a capacitor with a lateral boundary such that a portion of the dielectric layer is disposed in an inter-electrode region 180. The inter-electrode region 180 is within the lateral boundary of the upper electrode 140 and between the lower electrode layer 120 and the upper electrode 140.



A portion of the exposed portion of the dielectric layer is subsequently removed to expose a portion of the lower electrode layer, whereby a portion of the dielectric layer is removed from the inter-electrode region 180. Appellants' patent application states, "An unwanted consequence of step 10 is that, as discussed in the background section, some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180" (Specification, p. 10, lines 28-30). A conformal insulating layer 170, as shown in figure 4 of Appellants' application, is subsequently formed over a portion of the exposed portion of the lower electrode layer 120 proximate to the portion of the dielectric layer that is disposed within the inter-electrode region 180, thereby forming a portion of the conformal insulating layer 170 within the inter-electrode region.

Then an anti-reflective layer (ARL) is formed over a portion of the conformal insulating layer 170 for use in a photolithographic process.

A. Independent claim 3[2]

Claim 3 recites a method of forming a capacitor in an integrated circuit comprising seven limitations. (a) Forming a lower electrode layer on a semiconductor body is disclosed in figure 2 as a lower electrode layer 120 on a field oxide or other underlying layer 130 (Specification, p. 9, lines 28-32) and by step 1 at line 4 of page 9. (b) Forming a dielectric layer over a portion of the lower electrode layer is disclosed in figure 3 by dielectric layer 160 (Specification, p. 10, lines 3-5) and by step 4 at line 8 of page 9. (c) Forming an upper electrode layer over a portion of the dielectric layer is disclosed in figure 2 by upper electrode 140 (Specification, p. 10, lines 13-15) and by step 5 at line 9 of page 9. (d) Removing a portion of the upper electrode layer to expose a portion of the dielectric layer is disclosed in figure 2 by upper electrode 140 (Specification, p. 10, lines 11-12) and by step 9 at line 13 of page 9. Figure 2 also discloses a portion of the dielectric layer 160 disposed in an inter-electrode region disposed within the lateral boundary of the upper electrode 140 and between the lower electrode layer 120 and the upper electrode 140. (e) In step 10 at line 14 of page 9, and as shown in figure 3, a portion of the exposed portion of the dielectric layer is removed to expose a portion of the lower electrode layer 120, and a portion of the dielectric layer is removed from the inter-electrode region 180 (Specification, p. 10, lines 28-30). (f) Forming a conformal insulating layer 170 over a portion of the exposed portion of the lower electrode layer 120 proximate to the portion of the dielectric layer 160 disposed in the inter-electrode region 180

[2] Since the filing of the Appeal Brief on June 21, 2004, the Rules as to the form of appeal briefs have changed (although the MPEP has not). In a Notification of Non-Compliant Appeal Brief dated June 10, 2005, the Supervisory Examiner states, "Further, in applicants 'summery of invention' it is not clear where each limitaiton of each independent claim is recited" (emphasis added). In response, Appellants provide the following explanation on a limitation-by-limitation basis.

is disclosed in figure 4 (Specification, p. 12, lines 1-18) and by step 10a at line 15 of page 9. Figure 4 shows that a portion of the conformal insulating layer 170 is formed in the inter-electrode region 170 (Specification, p. 12, lines 8-10).
(g) Forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of the conformal insulating layer 170 is disclosed in figure 5 by anti-reflective layer 190 (Specification, p. 12, lines 19-20) and by step 11 at line 17 of page 9.

B. Independent claim 36

Claim 36 recites a method of forming an integrated circuit comprising six limitations. (a) Forming a conductive layer 120 on a semiconductor body 130 is disclosed in figure 2 (Specification, p. 9, lines 28-32) and by step 1 at line 4 of page 9. (b) Forming a capacitor structure by forming a top electrode 140 and a dielectric layer 160 is disclosed in figure 2 and in steps 5 and 4, respectively (Specification, p. 9, lines 8-9; p. 10, lines 3-5 and 13-15). (c) Forming a conformal insulating layer 170 over the capacitor structure such that a portion of the conformal insulating layer 170 is formed in an inter-electrode region 180 within the lateral boundary of the top electrode is disclosed in figure 4 (Specification, p. 12, lines 1-18) and by step 10a at line 15 of page 9.
(d) Forming an anti-reflective layer 190 for use in a photolithographic process over a portion of the conformal layer 170 is disclosed in figure 5 (Specification, p. 12, lines 19-20) and by step 11 at line 17 of page 9. (e) Forming a patterned mask over the anti-reflective layer 190 is disclosed at lines 20-22 on page 12 of the specification and by step 12 at line 18 of page 9. (f) Etching the conductive layer 120 using the patterned mask is disclosed at lines 20-22 on page 12 of the specification and by step 13 at line 19 of page 9.

C. Independent claim 103

Claim 103 recites a method comprising six limitations. (a) Forming a lower electrode layer 120 upon an underlying layer 130 of a semiconductor

device is disclosed in figure 2 (Specification, p. 9, lines 28-32) and by step 1 at line 4 of page 9. (b) Forming a capacitor dielectric layer 160 disposed in an inter-electrode region 180 between the lower electrode layer 120 and an upper electrode layer 140 is disclosed in figure 3 (Specification, p. 10, lines 3-5) and by step 4 at line 8 of page 9. (c) Forming the upper electrode layer 140 is disclosed in figure 2 (Specification, p. 10, lines 13-15) and by step 5 at line 9 of page 9. (d) Removing a portion of the upper electrode layer 140 such that an upper electrode 140 is formed having an edge is disclosed in figure 2 (Specification, p. 10, lines 11-12) and by step 9 at line 13 of page 9. (e) Removing a portion of the dielectric layer 160 such that an exposed portion of the lower electrode layer 120 is formed and such that an undercutting 180 is formed in the inter-electrode region 180 underneath the edge of the upper electrode 140 is disclosed in figure 2 (Specification, p. 10, lines 26-30) and by step 9 at line 13 of page 9. Figure 2 shows that the dielectric layer 160 is absent from the undercutting 180. (f) Providing a conformal insulating layer 170 over the upper electrode 140 and over the exposed portion of the lower electrode layer 120 such that the undercutting 180 is filled in by the conformal insulating layer 170 is disclosed in figure 4 (Specification, p. 12, lines 1-18) and by step 10a at line 15 of page 9. (g) Providing an anti-reflective layer 190 over the conformal insulating layer 170 is disclosed in figure 5 (Specification, p. 12, lines 19-20) and by step 11 at line 17 of page 9.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following are grounds of rejection to be reviewed on appeal:

1) The Examiner rejected claims 3, 8-11, 36, 39, 74 and 102-105 under 35 U.S.C. § 103 as being unpatentable over Takahashi (USP 5,683,931) in view of Watanabe (USP 6,225,658), Pfiester (USP 4,966,864) and Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology,

March 1997, p. 109). On appeal, the Board of Patent Appeals and Interferences (the "Board") is to review whether to reverse this decision of the Examiner.

2) The Examiner rejected claims 4-7, 37-38 and 106 under 35 U.S.C. §103 as being unpatentable over Takahashi, Watanabe, Pfiester and Bencher, in further view of Wang et al. (USP 5,545,585). On appeal, the Board is to review whether to reverse this decision of the Examiner.

3) The Examiner rejected claims 72-73 under 35 U.S.C. §103 as being unpatentable over Takahashi, Watanabe, Pfiester and Bencher, in further view of Jain et al. (USP 5,741,626). On appeal, the Board is to review whether to reverse this decision of the Examiner.

4) The Examiner has required Appellants to label figures 2 and 3 as "Prior Art" in order to avoid abandonment of the application. (Office Action, p. 3, lines 6-9) On appeal, the Board is to review whether the Examiner can force Appellants to label figures 2 and 3 as "Prior Art" when, in fact, figures 2 and 3 do not depict the prior art.

VII. ARGUMENT

A. Claims 3, 8-11, 36, 39, 72-74 and 102-105 (1st ground of rejection)

In the previous office action dated January 20, 2004, the Examiner rejected claims 3, 8-11, 36, 39, 72-74, 102-105 and 107-108 under 35 U.S.C. §103 for being rendered obvious over a three-way combination of Takahashi (USP 5,683,931), art that the Examiner characterized as "Applicant's admitted prior art (AAPA)", and Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109). Claims 107-108 are not the subject of this Appeal because they were cancelled in the amendment that accompanied Appellants' first appeal brief dated June 21, 2004. In the current Office Action, the Examiner substitutes Watanabe (USP 6,225,658) and Pfiester (USP 4,966,864) for the AAPA. The Examiner now rejects claims 3, 8-

11, 36, 39, 72-74, 102-105 and 107-108 under 35 U.S.C. §103 for being rendered obvious over a four-way combination of Takahashi, Watanabe, Pfiester and Bencher.

The Examiner rejects each of independent claims 3, 36 and 103 with substantially the same argument.

i. Independent claim 3.

Independent claim 3 has seven elements (a) through (g): "(a) forming a lower electrode layer on a semiconductor body; (b) forming a dielectric layer over a portion of said lower electrode layer; (c) forming an upper electrode layer over a portion of said dielectric layer; (d) removing a portion of said upper electrode layer to expose a portion of said dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of said dielectric layer is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary of said upper electrode and between said lower electrode layer and said upper electrode; (e) subsequently removing a portion of said exposed portion of said dielectric layer to expose a portion of said lower electrode layer, wherein a portion of said dielectric layer is removed from said inter-electrode region; (f) subsequently forming a conformal insulating layer over a portion of said exposed portion of said lower electrode layer proximate to said portion of said dielectric layer disposed in said inter-electrode region, whereby a portion of conformal insulating layer is formed in said inter-electrode region; and (g) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal insulating layer."

The Examiner states, with regard to claim 3, that Takahashi discloses elements (a), (b), (c) and (d). The Examiner admits that Takahashi does not disclose element (e):

> "Takahashi discloses in figure 2c subsequently removing a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode layer. Takahashi is silent to a method of etching this

process step and wherein a portion of the dielectric layer is removed from the inter-electrode region." (Office Action, p. 4, lines 9 – 13)

The Examiner introduces Watanabe with regard to claim 3, but admits that Watanabe also does not disclose element (e):

"Watanabe teaches in figures 2c and 2d, and column 5, lines 54-62, specifically line 60, a method of etching a capacitor dielectric layer (10) using wet etching. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the wet etching of Watanabe in the method of Takahashi in order to use an etching process that is well understood in the art. It is not clear that Takahashi and Watanabe teach wherein a portion of the dielectric layer is removed from an inter-electrode region." (Office Action, p. 4, lines 13 – 18)

Still with regard to claim 3, the Examiner introduces Pfiester. But the Examiner does not state that Pfiester discloses element (e). Instead, the Examiner asserts that it would have been obvious to combine Pfiester with Watanabe and Takahashi to arrive at element (e):

"Pfiester teaches in figure 2 and column 3, lines 12-15 wherein an undercutting occurs during wet etching. It would have been obvious to one of ordinary skill in the art at the time of the invention that a portion of the dielectric layer is removed from an inter-electrode region while using the wet etch of Watanabe in the method of Takahashi because undercutting is a property of wet etch as taught by Pfiester in figure 2 and column 3, lines 12-15. It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region of Watanabe

and Pfiester in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20-23, of Takahashi using a process well known as suggested by the cited sections of Watanabe and Pfiester." (Office Action, p. 4, line 21 – p. 5, line 5)

Still with regard to claim 3, the Examiner asserts that it would have been obvious to combine Pfiester with Watanabe and Takahashi to arrive at element (f):

"Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over a portion of the exposed portion of the lower electrode layer proximate to the portion of the dielectric layer disposed in the inter-electrode region. It would have been further obvious in the method of Takahashi, Watanabe, and Pfiester whereby a portion of the conformal insulating layer is formed in the inter-electrode region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer." (Office Action, p. 5, lines 5 – 11)

The Examiner then admits that the hypothetical Takahashi/Watanabe/ Pfiester combination fails to include an anti-reflective layer of element (g). The Examiner therefore cites another reference, Bencher, and states:

"Takahashi, Watanabe, and Pfiester are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill

> in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi and the AAPA in order to improve the photolithographic mask in the method of Takahashi, Watanabe, and Pfiester in order to improve the photolithographic process by reducing net linewidth variations as is well known in the art." (Action, p. 5, lines 11 – 20)

ii. Independent claim 36.

Independent claim 36 has six elements: "(a) forming a conductive layer on a semiconductor body; (b) forming a capacitor structure, comprising: a top electrode over a portion of said conductive layer, wherein said top electrode has a lateral boundary; and a dielectric layer between said top electrode and said conductive layer; (c) forming a conformal insulating layer over said capacitor structure and a portion of said conductive layer proximate to said capacitor structure, wherein a portion of said conformal insulating layer is formed in an inter-electrode region within said lateral boundary of said top electrode and between said top electrode and said conductive layer; (d) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal layer; (e) forming a patterned mask over said anti-reflective layer (ARL); and (f) etching said conductive layer using said patterned mask."

With regard to claim 36, the Examiner asserts that it would have been obvious to combine Pfiester with Watanabe and Takahashi to arrive at element (c):

> "Pfiester teaches in figure 2 and column 3, lines 12-15 wherein an undercutting occurs during wet etching. It would have been obvious to one of ordinary skill in the art at the time of the invention that a portion of the dielectric layer is removed from an inter-electrode region within the lateral boundary of the top electrode and between the top

electrode and the conductive layer while using the wet etch of Watanabe in the method of Takahashi because undercutting is a property of wet etch as taught by Pfiester in figure 2 and column 3, lines 12-15. It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region within the lateral boundary of the top electrode and between the top electrode and the conductive layer of Watanabe and Pfiester in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20-23, of Takahashi using a process well known as suggested by the cited sections of Watanabe and Pfiester." (Office Action, p. 6, line 21 – p. 7, line 10)

iii. Independent claim 103.

Independent claim 103 has seven elements: "(a) forming a lower electrode layer upon an underlying layer of a semiconductor device; (b) forming a capacitor dielectric layer; (c) forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer; (d) removing a portion of said upper electrode layer such that an upper electrode is formed having an edge; (e) removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed and such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting; (f) providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer such that said undercutting is filled in by said conformal insulating layer; and (g) providing a anti-reflective layer over said conformal insulating layer."

With regard to claim 103, the Examiner asserts that it would have been obvious to combine Pfiester with Watanabe and Takahashi to arrive at element (f):

> "Pfiester teaches in figure 2 and column 3, lines 12-15 wherein an undercutting occurs during wet etching. It would have been obvious to one of ordinary skill in the art at the time of the invention that a portion of the dielectric layer is removed and an undercutting is formed underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting from an inter-electrode region while using the wet etch of Watanabe in the method of Takahashi because undercutting is a property of wet etch as taught by Pfiester in figure 2 and column 3, lines 12-15. It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting of Watanabe and Pfiester in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20-23, of Takahashi using a process well known as suggested by the cited sections of Watanabe and Pfiester." (Office Action, p. 9, lines 8 – 20)

Appellants' Response

The Examiner rejects claims 3, 8-11, 36, 39, 74 and 102-105 under 35 U.S.C. §103 as being obvious over a four-way combination of Takahashi, Watanabe, Pfiester and Bencher. Claims 3, 36 and 103 are independent claims, and the remaining claims listed above depend from those claims. The Examiner's rejection should be withdrawn because at least one element of each of independent claims 3, 36 and 103 is not disclosed in any of Takahashi, Watanabe, Pfiester or Bencher. Parts of element (f) of claim 3, element (c) of

claim 36, and element (f) of claim 103 recite a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting.

The Examiner has not established a *prima facie* case of obviousness. The MPEP § 2142 states:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the reference (or references when combined) must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. . . . 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.' Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)" (emphasis added). MPEP § 2142.

Nowhere does any of Takahashi, Watanabe, Pfiester or Bencher disclose a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Moreover, the Examiner has not identified suggestions or motivations in Takahashi, Watanabe, Pfiester or Bencher that would motivate one of ordinary skill in the art to combine Takahashi, Watanabe, Pfiester and Bencher in a particular way that would result in a conformal insulating layer being filled, provided or formed in an inter-electrode region or in an undercutting. The Examiner has not identified a motivation to combine Takahashi with Watanabe

and then a motivation to combine the combination Takahashi/Watanabe with Pfiester, and then a motivation to combine the combination Takahashi/ Watanabe/Pfiester with Bencher.

i. All claim limitations are not taught.

The Examiner does not contend that any of Takahashi, Watanabe, Pfiester or Bencher discloses the limitation of a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Not only does Pfiester not disclose an undercutting, it does not disclose an undercutting filled with an insulating layer. Rather, Pfiester discloses a conductive "bridge 26 which electrically couples polycrystalline silicon electrode 16 and substrate 12" (Pfiester, col. 3, lines 24-26). Thus, the inventions of claims 3, 36 and 103 are unobvious over the cited references because the cited references, even when combined, do not teach or suggest the claimed limitation of a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Thus, the Examiner has not established the third criteria of a *prima facie* case of obviousness.

Although the references do not disclose forming a portion of a conformal insulating layer in an inter-electrode region (the third criteria of a prima facie case of obviousness), the Examiner nevertheless argues that it would have been obvious in the method of Takahashi, Watanabe, and Pfiester to form a portion of a conformal insulating layer in an inter-electrode region. The Examiner does not state that the references expressly or impliedly suggest combining themselves in the particular manner and order so as to obtain a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Indeed, the references do not expressly or impliedly suggest performing various step of Takahashi, then performing a step of Watanabe, then recognizing a condition of Pfiester, then performing another step of Takahashi and then performing a step of Bencher. Nor does the Examiner present a convincing line of reasoning as to why one or ordinary skill in the art would have been led to combine the multiple

teachings of the references in the particular manner and order to arrive at the claimed inventions. The Examiner simply repeats "it would have been obvious" and then inserts the various parts of the elements of claim 3, 36 or 103. The Examiner does not present any line of reasoning. Thus, the Examiner has not established the first criteria of a *prima facie* case of obviousness.

ii. No motivation to combine references to obtain the inventions.

Appellants contend that no line of reasoning would lead to a motivation to perform various step of Takahashi and then a step of Watanabe in order to create a condition for a potential problem (the problem being related to a condition of Pfiester but nevertheless unrecognized by Pfiester), then to perform another step of Takahashi in order to prevent the unrecognized problem from occurring when a step of Bencher is performed. This complicated sequence would not have been obvious to one of skill in the art.

In fact, Pfiester teaches away from recognizing that an undercutting condition, when combined with other teachings, could result in a problem. The problem solved by Pfiester is entirely unrelated to undercutting:

> "If the opening 22 is etched using a wet etchant or other isotropic etchant, some undercutting of photoresist pattern 20 and electrode 16 will be observed, as illustrated in FIG. 2. If an anisotropic etchant is used, no undercutting will be observed and the resultant opening will be more like that illustrated by the dashed lines 24. The type of etchant used to etch the contact opening, whether wet, dry, isotropic or anisotropic, is not material to the practice of the invention" (Pfiester, col. 3, lines 12 – 21) (emphasis added).

iii. No reasonable expectation of success.

Although the Examiner does not provide any line of reasoning as to why one of skill in the art would have combined Takahashi, Watanabe, Pfiester and Bencher in a manner and order that might have resulted in a conformal insulating

layer filled, provided or formed in an inter-electrode region or in an undercutting, the Examiner does identify one motivation to combine Bencher with a myriad of other references. Randomly combining Bencher with a myriad of references, however, on the chance of happening to combine it with a hypothetical combination of Takahashi/ Watanabe/Pfiester would not have resulted in a reasonable expectation of obtaining a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. Thus, the Examiner has not established the second criteria of a *prima facie* case of obviousness.

The Examiner identifies a motivation "to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi, Watanabe, and Pfiester in order to improve the photolithographic process by reducing net linewidth variations as is well known in the art." (Office Action, p. 5, lines 16 – 20). The motivation identified by the Examiner is not a motivation to combine Bencher specifically with Takahashi, Watanabe, and Pfiester, but rather is only a motivation to combine Bencher with references that seek to solve the problem of excessive variation in net linewidths. That problem is not peculiar to a hypothetical combination of Takahashi, Watanabe, and Pfiester. One of ordinary skill in the art, who was confronted with the problem of reducing net linewidth variations, would not have been motivated to combine Bencher with one particular reference any more than with a myriad of other references. And there would have been no particular motivation to combine Bencher with the hypothetical combination of Takahashi and Watanabe and Pfiester. Moreover, one of ordinary skill in the art, who was confronted with the problem of capacitor leakage, would not have been motivated to combine the hypothetical combination of Takahashi and Watanabe and Pfiester with Bencher because reducing net linewidth variation was not a primary consideration in solving the problem of capacitor leakage. Finally, as explained in detail below, one of ordinary skill in the art given the hypothetical combination of Takahashi/ Watanabe/Pfiester would not even have been confronted with the problem of

capacitor leakage because the capacitor leakage occurs through the anti-reflective layer of Bencher.

Admittedly, the Federal Circuit has held that "[a]s long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor." In re Beattie, 974 F.2d 1309, 1312, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992). See also In re Dillon, 919 F.2d 688, 693, 16 USPQ2d 1879, 1901 (Fed. Cir. 1990), cert. denied., 500 U.S. 904 (1991). In this case, however, the Appellants' inventions include the discovery of the source of a problem, namely that the existence of undercutting increases leakage current in capacitors when they are covered by anti-reflective layers. "[W]here the claimed invention solves a problem, the discovery of the source of the problem and its solution are considered to be part of the 'invention as a whole' under 35 U.S.C. 103." Ex parte Hiyamizu, 10 USPQ2d 1393, 1394-5, (Bd.Pat.App & Interf. Apr 28, 1998), citing In re Kaslow, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983) and In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1979) ("[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified.")

In the present case, it is not pertinent whether the combination of Takahashi, Watanabe, Pfiester and Bencher also has the attribute of solving another problem not confronted by the inventors. There still must be evidence that a "skilled artisan, confronted with the same problem as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998) (emphasis added). One of ordinary skill in the art would not have been motivated to combine Takahashi, Watanabe, Pfiester and Bencher to solve the problem of current leaking through an anti-reflective layer from one capacitor plate to another. One of ordinary skill in the art would not have been inclined to use the teaching of Bencher (which discloses an anti-reflective layer) to solve the problem identified by the inventors

because the identified problem does not occur unless an anti-reflective layer is used. The Examiner admits that "Takahashi, Watanabe, and Pfiester are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer" (Office Action, p. 5, lines 11 – 13). So the identified problem that results from an antireflective layer would not have presented itself to one of ordinary skill in the art who was in possession of the teachings of Takahashi, Watanabe, and Pfiester.

It is improper for the Examiner to base a *prima facie* case of obviousness on a motivation to combine a last reference (Bencher) with a combination of references (Takahashi/Watanabe/Pfiester) where the motivation to form the combination of references would not have arisen without the last reference. To do so impermissibly defines the problem in terms of its solution. "Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness." Monarch Knitting Mach. Corp. V. Sulzer Morat GmbH, 139 F.3d 877, 880, 45 USPQ2d 1977, 1981 (Fed. Cir. 1998). See also Ecolochem Inc. V. Southern California Edison, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000). The motivation to perform a step of Takahashi (forming a conformal insulating layer after having recognized a condition of Pfiester and after having performed various other steps of Takahashi) would not have existed without capacitor leakage caused by a step of Bencher. It is improper for the Examiner to base an obviousness rejection on a motivation to combine a reference that results from a problem other than the problem facing the inventors where the problem facing the inventors would not have existed but for the element or step taught by the reference. Inasmuch as a patentable invention may lie in the discovery of the source of a problem, one of skill in the art and in possession of the teachings of Takahashi, Watanabe, Pfiester and Bencher would never have arrived at the Appellants' inventions because the problem identified by the inventors would not have existed given the motivation identified by the Examiner for combining Bencher with a combination of Takahashi/Watanabe/Pfiester.

Claims 8-11, 74 and 102 depend directly or indirectly from claim 3. Appellants respectfully submit that claims 8-11, 74 and 102 are allowable for at least the same reasons for which claim 3 is allowable. Allowance of claims 8-11, 74 and 102 is requested.

Claim 39 depends from claim 36. Appellants respectfully submit that claim 39 is allowable for at least the same reasons for which claim 39 is allowable. Allowance of claim 39 is requested.

Claims 104-105 depend from claim 103. Appellants respectfully submit that claims 104-105 are allowable for at least the same reasons for which claim 103 is allowable. Allowance of claims 104-105 is requested.

Therefore, the §103 rejection of claims 3, 8-11, 36, 39, 74 and 102-105 as being unpatentable under 35 U.S.C. §103 over Takahashi, Watanabe, Pfiester and Bencher should be withdrawn. Appellants respectfully submit that these claims are allowable.

B. Claims 4-7, 37-38 and 106 (2nd ground of rejection)

The Examiner rejects claims 4-7, 37-38 and 106 under 35 U.S.C. §103 for being rendered obvious over a five-way combination of Takahashi, Watanabe, Pfiester, Bencher and Wang et al. (USP 5,545,585). Just as the Examiner presents no convincing line of reasoning under Issue 1 above as to why one or ordinary skill in the art would have combined the teachings of Takahashi, Watanabe, Pfiester and Bencher, the Examiner also provides no line of reasoning to combine five references in the particular manner and order to arrive at the inventions of claims 4-7, 37-38 and 106.

In addition, claims 4-7 depend directly or indirectly from claim 3. Thus, dependent claims 4-7 are allowable for at least the same reasons explained above for which claim 3 is allowable. Claims 37-38 depend directly from claim 36. Claims 37-38 are therefore allowable for at least the same reasons explained above for which claim 36 is allowable. Claim 106 depends directly on claim 103 and is, therefore, allowable for at least the same reasons explained

above for which claim 103 is allowable.

C. Claims 72-73 (3rd ground of rejection)

The Examiner rejects claims 72-73 under 35 U.S.C. §103 for being rendered obvious over a five-way combination of Takahashi, Watanabe, Pfiester, Bencher and Jain et al. (USP 5,741,626). The Examiner provides no line of reasoning as to why one of skill in the art would have combined these five references in the particular manner and order to arrive at the inventions of claims 72-73. Claims 72-73 depend directly or indirectly from claim 3. Thus, dependent claims 72-73 are allowable for at least the same reasons explained above for which claim 3 is allowable.

D. Figures 2 and 3 do not depict prior art (4th ground to be reviewed)

Issue No. 2 of Appellants' first appeal brief dated June 21, 2004, concerned "[w]hether the Examiner can force Appellants to label figures 2 and 3 as "Prior Art" and whether the Examiner has incorrectly characterized as "Applicant's admitted prior art (AAPA)" the Appellants' recognition that the undercutting is the source of a problem." The office action dated January 20, 2004, contained rejections under 35 U.S.C. § 103 based on various references plus the AAPA. In the Office Action, however, the Examiner has now substituted two new references in place of the AAPA referred to in the office action dated January 20, 2004.

Although all references to the AAPA have been removed from the Office Action, the first six paragraphs of the Office Action remain identical to the first six paragraphs of the office action dated January 20, 2004. The objection in paragraph six still requires Appellants to label figures 2 and 3 as "Prior Art." The Examiner repeats that "Figures 2 and 3 should be designated by a legend such as –Prior Art— . . . A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application" (Office Action, page 3, lines 6-8) (emphasis added).

The objection to figures 2 and 3 now has no supporting argument and constitutes an artifact of an abandoned position. The argument Appellants presented in the first appeal brief dated June 21, 2004, as to why figures 2 and 3 do not depict prior art remains valid. The teachings in Appellants' application specification of (a) the existence of undercutting in an inter-electrode region, and (b) a problem associated with undercutting when the structure is covered by an anti-reflective layer (ARL) do not appear in a section of Appellants' specification entitled "PRIOR ART." Instead, the section is called "Background of the Invention." Appellants' patent application states, "Figure 2 shows an embodiment of the present invention at the state where the upper electrode has been defined. Figure 3 shows the same embodiment after the excess capacitor dielectric has been removed" (Application specification, page 7, lines 26-29). Appellants' patent application also states, "An unwanted consequence of step 10 is that ... some of the wanted dielectric is also removed. This is the undercutting indicated in Figure 3 at 180" (Application specification, page 10, lines 28-30). Appellants state for the record that the problem they have identified is not prior art. Figures 2 and 3 were not designated by a legend such as "Prior Art" because they do not depict prior art but rather the source of a problem identified by Appellants and solved by the Appellants' inventions.

The objection to Figures 2 and 3 should be withdrawn.

E. Claim 102

Appellants note that the rejection of claim 102 under 35 U.S.C. §112 that appeared in the office action dated January 20, 2004, does not appear in the Office Action. The Examiner had previously argued that claim 102 fails to meet the written description requirement under 35 U.S.C. §112, first paragraph, because the claim recites "using isotropic wet etching." Issue 4 of the first appeal brief dated June 21, 2004, concerned "[w]hether claim 102 fails to meet the written description requirement under 35 U.S.C. §112, first paragraph, because the claim recites "using isotropic wet etching."

VIII. FEES

Prosecution was reopened prior to a decision on the merits by the Board of Patent Appeals and Interferences. Thus, Appellants request that the fees paid by Appellants for the notice of appeal, the appeal brief, and the request for oral hearing be applied to this reinstated appeal on the same application. See MPEP §1208.02 Reopening of Prosecution After Appeal.

IX. CONCLUSION

The Examiner has not established a *prima facie* case of obviousness. Each of the claims 3-11, 36-39, 72-74, 102-106 recites a conformal insulating layer filled, provided or formed in an inter-electrode region or in an undercutting. This structural feature is not disclosed in any reference cited by the Examiner. The discovery that undercutting is a source of the problem of current leaking through an anti-reflective layer from one capacitor plate to another is part of Appellants' inventions. The source of the problem identified by Appellants is nowhere recognized in the cited prior art. Moreover, the Examiner has not identified a motivation or suggestion to combine either (i) all of the four references that are the basis for the rejection of claims 3, 8-11, 36, 39, 72-74 and 102-105 or (ii) all of the five references that are the basis for the rejection of claims 4-7, 37-38 and 106. Therefore, Appellants respectfully request that the Board reverse the rejections of pending claims 3-11, 36-39, 72-74 and 102-106 and allow all pending claims.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By 
Darien K. Wallace

Date of Deposit: June 21, 2005

Respectfully submitted,

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X. CLAIMS APPENDIX

Claims 1 – 2 (canceled)

3. (previously presented): A method of forming a capacitor in an integrated circuit comprising:

(a) forming a lower electrode layer on a semiconductor body;

(b) forming a dielectric layer over a portion of said lower electrode layer;

(c) forming an upper electrode layer over a portion of said dielectric layer;

(d) removing a portion of said upper electrode layer to expose a portion of said dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of said dielectric layer is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary of said upper electrode and between said lower electrode layer and said upper electrode;

(e) subsequently removing a portion of said exposed portion of said dielectric layer to expose a portion of said lower electrode layer, wherein a portion of said dielectric layer is removed from said inter-electrode region;

(f) subsequently forming a conformal insulating layer over a portion of said exposed portion of said lower electrode layer proximate to said portion of said dielectric layer disposed in said inter-electrode region, whereby a portion of conformal insulating layer is formed in said inter-electrode region; and

(g) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal insulating layer.

4. (previously presented): The method of claim 3, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

5. (previously presented): The method of claim 3, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

6. (previously presented): The method of claim 5, wherein said thermal process is a rapid thermal oxidation (RTO) performed for a length of time ranging from 10 to 60 seconds and at a temperature ranging from 850°C to 1050°C.

7. (previously presented): The method of claim 3, wherein said conformal insulating layer is formed by deposition.

8. (original): The method of claim 3, wherein said ARL is an anti-reflective coating.

9. (original): The method of claim 3, wherein said ARL is titanium nitride.

10. (original): The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. (previously presented): The method of claim 10, wherein said plasma enhanced chemical vapor deposition anti-reflective layer (PEARL) has a thickness ranging from 300 angstroms to 400 angstroms.

Claims 12 – 35 (canceled)

36. (previously presented): A method of forming an integrated circuit comprising:

(a) forming a conductive layer on a semiconductor body;

(b) forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer, wherein said top electrode has a lateral boundary; and

a dielectric layer between said top electrode and said conductive layer;

(c) forming a conformal insulating layer over said capacitor structure and a portion of said conductive layer proximate to said capacitor structure, wherein a portion of said conformal insulating layer is formed in an inter-electrode region within said lateral boundary of said top electrode and between said top electrode and said conductive layer;

(d) forming an anti-reflective layer (ARL) for use in a photolithographic process over a portion of said conformal layer;

(e) forming a patterned mask over said anti-reflective layer (ARL); and

(f) etching said conductive layer using said patterned mask.

37. (previously presented): The method of claim 36, wherein said conformal insulating layer has a thickness ranging from 20 angstroms to 70 angstroms.

38. (previously presented): The method of claim 36, wherein said conformal insulating layer is an oxide layer formed in a thermal process.

39. (previously presented): The method of claim 36, wherein said conductive layer is additionally used to form a gate of one or more transistors formed on said integrated circuit.

Claims 40 – 71 (canceled)

72. (previously presented): The method of claim 3, further comprising:

(h) forming a photoresist mask over a portion of said anti-reflective layer (ARL); and

(i) irradiating said photoresist mask with radiation that penetrates said photoresist mask, wherein said anti-reflective layer reduces a reflection of said radiation by 70% or more.

73. (previously presented): The method of claim 72, wherein the anti-reflective layer reduces said reflection of said radiation by 70% to 85%.

74. (previously presented): The method of claim 3, wherein said anti-reflective layer is a SixONy film.

Claims 75 – 101 (canceled)

102. (previously presented): The method of claim 3, wherein said subsequently removing a portion of said exposed portion of said dielectric layer in step (e) is performed using isotropic wet etching.

103. (previously presented): A method comprising:

(a) forming a lower electrode layer upon an underlying layer of a semiconductor device;

(b) forming a capacitor dielectric layer;

(c) forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer;

(d) removing a portion of said upper electrode layer such that an upper electrode is formed having an edge;

(e) removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed and such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting;

(f) providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer such that said undercutting is filled in by said conformal insulating layer; and

(g) providing a anti-reflective layer over said conformal insulating layer.

104. (previously presented): The method of claim 103, wherein the forming in step (b) is performed by depositing said capacitor dielectric layer to a thickness ranging from 300 angstroms to 800 angstroms.

105. (previously presented): The method of claim 103, wherein said underlying layer electrically isolates said lower electrode layer.

106. (previously presented): The method of claim 103, wherein the providing the conformal insulating layer in step (f) is performed using a rapid thermal oxidation (RTO) process to grow a layer of silicon oxide to a thickness ranging from 20 angstroms to 100 angstroms.

Claims 107 – 108 (canceled)

109. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed within an inter-electrode region, said inter-electrode region disposed within said lateral boundary between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

a conformal layer of an insulating material disposed over said upper electrode and over said exposed portion of said lower electrode layer;

an undercutting in said inter-electrode region, wherein said capacitor dielectric is absent from said undercutting and said undercutting is filled by said insulating material; and

an anti-reflective layer disposed over said conformal layer of said insulating material.

110. (withdrawn): The device of claim 109, wherein said anti-reflective layer is titanium nitride.

111. (withdrawn): The device of claim 109, wherein said anti-reflective layer is a plasma enhanced anti-reflective layer (PEARL).

112. (withdrawn): The device of claim 109, wherein said lower electrode layer is polysilicon.

113. (withdrawn): A device comprising:

a lower electrode layer disposed on an underlying layer of a semiconductor substrate;

a capacitor dielectric disposed on said lower electrode layer;

an upper electrode disposed on said capacitor dielectric, wherein said upper electrode has a lateral boundary, wherein said capacitor dielectric is disposed in an inter-electrode region, said inter-electrode region disposed within said lateral boundary and between said lower electrode layer and said upper electrode layer, and wherein an exposed portion of said lower electrode layer lies outside said lateral boundary;

an anti-reflective layer disposed over said upper electrode and over said exposed portion of said lower electrode layer; and

means for preventing an electrical connection through said anti-reflective layer from said upper electrode to said lower electrode layer, wherein said means is at least partially disposed within said inter-electrode region.

114. (withdrawn): The device of claim 113, wherein said anti-reflective layer is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

XI. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132. No affidavit or declaration has been submitted under § 1.130 to disqualify a commonly owned patent or a published application as prior art. No affidavit or declaration of a prior invention has been submitted under § 1.131. No affidavit or declaration traversing rejections or objections has been submitted under § 1.132. No such evidence was entered by the Examiner and relied upon by Appellants in this appeal.

In the rejections that are the grounds to be reviewed in this appeal, the Examiner has relied upon only one non-patent document: Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109), a copy of which is attached. The Examiner cites Bencher at lines 20-21 of page 3 of the Office Action.

XII. RELATED PROCEEDINGS APPENDIX

No decision has yet been rendered by a court or the Board in this or any related proceeding.

N C

9-11-02
OA

Title: *DIELECTRIC ANTIREFLECTIVE COATINGS FOR DUV LITHOGRAPHY* , By: Bencher, Christopher, Ngai, Chris, Solid State Technology, 0038111X, Mar97, Vol. 40, Issue 3
Database: *Business Source Corporate*

Section: MATERIALS

DIELECTRIC ANTIREFLECTIVE *COATINGS* FOR *DUV LITHOGRAPHY*

Contents

High performance plasma-enhanced chemical vapor deposition (PECVD) ***dielectric*** antireflective ***coatings*** (ARC) can be readily designed by combining theoretical models from photolithography simulators with the manufacturing capabilities of silane-based plasma deposition chambers. By following the three steps outlined, the design of these ARCs can be made available to any semiconductor manufacturer for numerous applications. This paper demonstrates how a ***dielectric*** ARC was designed for aluminum metallization at ***DUV*** (248-nm) wavelengths. This ARC had <3% CD swing and <2% within-wafer linewidth uniformity variation.

While ARCs have been used to enhance IC ***lithography*** for years, the CD budget allowed in advanced sub-0.35-mum ***lithography*** is plating more demands on them. Design specifications of next-generation devices will require ARCs to suppress >99% of substrate-reflected light, meet stringent photoresist and device contamination requirements, and operate at extended ultraviolet wavelengths. Many of these requirements are not met by the conventional ARCs in production today.

During photolithography, light from the stepper is passed through a mask and the pattern is transferred to the wafer coated with photoresist. However, when the underlying film is highly reflective, as in metal and polysilicon layers, light reflections can destroy the pattern resolution by three mechanisms: a) off-normal incident light can be reflected back through the resist that is intended to be masked; b) incident light can be reflected off device features and expose "notches" in the resist; and c) thin-film interference effects can lead to linewidth variations when resist thickness changes are caused by wafer topology or nonflatness (Fig. 1) [1].

Over the past decade, semiconductor manufacturers have used many types of ARCs. These include bottom antireflective ***coatings*** beneath the photoresist to reduce substrate reflections, and top antireflective ***coatings*** deposited over the resist to reduce second-order reflections. Some photoresists have even been dyed in an attempt to absorb reflections [2]. Bottom ARC has emerged as the most effective in reducing reflections, while interfering the least with the photolithography process. However, with feature sizes shrinking well below 0.35 mum, and stepper projection systems shifting to shorter wavelengths, many conventional bottom ARCs no longer maintain acceptable linewidth variations.

In recent years, several semiconductor manufacturers have proposed the use of CVD-deposited ***dielectric*** films as antireflective layers that can meet the requirements of sub-0.35-mum photolithography [3-7]. CVD processes allow film stoichiometry and optical properties to be easily tuned to specific needs, while also reaping the benefits of a conformal layer. These ***dielectric*** ARCs can be used for extending i-line ***lithography***, or enabling ***DUV lithography***. As alternatives to organic spin-on ARC, they have applications ranging from polysilicon gate to metal layer patterning.

CVD-deposited ***dielectric*** ARCs work by phase-shift cancellation of specific wavelengths (Fig. 2). This requires the simultaneous specification of three optical parameters: refractive index n, extinction coefficient

k, and thickness d. Proper choice of these three parameters ensures that the transmitted wave that passes through the ARC film will, on reflection from the substrate, be equal in amplitude and opposite in phase to the wave reflected from the resist-ARC interface. In practice, phase cancellation requires very tight control of process parameters such that, for example, the thickness of the ARC is maintained to within 15 A.

In contrast, conventional spin-on organic bottom ARCs rely on the absorption of reflected light through a relatively thick film (1000-2000A). Further thickness increases occur at patterned steps because of the self-planarizing nature of spin-on films. As a result, the necessary nonselective overetch during the ARC breakthrough etch produces CD control problems. Conversely, CVD-deposited ***dielectric*** ARCs are thin (200-300A), conformal to device features, and usually very selective during the ARC etch, so that CD control is easily maintained during pattern transfer (Fig. 3).

Dielectric ARC design

To demonstrate design of a near-zero reflectivity ***dielectric*** ARC film for any application, we will examine the case of an ARC film for aluminum at ***DUV*** wavelengths. Bare aluminum can have reflectivities of >90% at ***DUV*** wavelengths, making it a difficult film to pattern. Additionally, traditional aluminum ARC layers, such as titanium nitride, may fail to meet the optical properties or resist contamination requirements demanded by ***DUV lithography*** [8,9].

Step 1. Simulation. The first step in the design of a high performance ARC is to determine the required optical properties (n, k, d) for total phase-shift cancellation. A desktop photolithography simulator, in this case Prolith/2 [10], can simplify optimization of the ARC for a given substrate film stack.

Typical simulation input variables include stepper parameters, mask pattern details, resist and developer types, and pre-and postexposure bake conditions. Of these parameters, only the wavelength, substrate film stack, and resist index of refraction are critical to the design of the ***dielectric*** ARC. These parameters will determine the substrate reflectivity, which can be minimized by adjusting the ***dielectric*** ARC optical constants n, k, and d. In the straightforward case of aluminum, neither the underlying film structures nor the aluminum film thickness plays a critical role, because the extinction coefficient of aluminum is high enough (2.35-2.94 k at 248 nm) so that any ***DUV*** will attenuate rapidly. The accurate predictions of resist profiles and CD control, however, require attention to all the input parameters. Second order effects, such as the angular distribution of substrate illumination, have not been considered in optimization of the ARC properties.

By running simulations in n, k, and d space, we can calculate substrate reflectivities at the resist-ARC interface and assemble contour maps (Fig. 4) to predict the performance of various ARC films. A reflectivity contour map, such as the one created here for aluminum films, is the primary tool needed to tune the CVD process to meet complete phase-shift cancellation conditions with the ***dielectric*** ARC film.

Step 2. Process targeting. Having established a substrate reflectivity contour map, we began to characterize a ***dielectric*** CVD process that could deliver n and k constants near a zero reflectivity contour. Silicon oxynitrides represented the best candidate ARC material family for several reasons. First, silicon oxynitrides possess an ideal range of optical properties that meet many simulation-targeted requirements (Fig. 5) [7]. Second, plasma-deposited SiO_xN_y has an amorphous structure and can, therefore, be fine-tuned to specific n and k requirements by varying the Si, O, and N contents of the film. Finally, silicon oxynitride films have been widely used in semiconductor manufacturing for years, and are compatible with most devices and process integration schemes.

This study used an Applied Materials single-wafer PECVD silane-based, lamp-heated chamber to tune the silicon oxynitride processes. To measure the wavelength-specific refractive indices and extinction coefficients of the deposited films, we used an n&k Analyzer [11-13], which also yields accurate measurements of film thickness.

By adjusting the gas flow ratios in the plasma, we developed n and k process trends intersecting with the reflectivity contour lines. Two such process trends were added to the contour map in Fig. 6. The recipes at the points of intersection between the process trends and the contour line of zero substrate reflectivity should, according to simulation, yield the highest performing ***dielectric*** ARCs.

We returned to the resist profile simulator to examine the performance differences of ***dielectric*** ARCs with

0%, 1%, and 3% substrate reflectivity. CD swing curve simulations [14] determined how well a resist linewidth will be maintained as the resist thickness varies, as with resist spun over device topography. Figure 7 predicts CD swing curves for ARCs with 0%, 1%, and 3% reflectivity, yielding swing ratios of <1%, 17%, and 30%, respectively. The ARC film designer can then balance the size of the acceptable PECVD process window in n, k, and d space with the allowable CD budget.

The sensitivity of the linewidth control to the substrate reflectivity (Fig. 7) illustrates the need for ultra-high performance ARCs when patterning with chemically amplified ***DUV*** photoresists. For processes requiring even modest CD budgets, ARC films will need to maintain consistent substrate reflectivities in the sub-1% range, placing tight constraints on the control of n, k, and d. The ability to accurately control the deposition of very thin films (zz250 A) is a fundamental advantage for PECVD ***dielectric*** ARCs in sub-0.35-pm ***lithography***.

Step 3. ***Lithography*** **testing.** Sample wafers were processed, patterned, and measured for CD swing control to verify the simulation predictions and test the ARC performance. Ten bare silicon wafers were deposited with 6000 A of blanket aluminum followed by a ***dielectric*** ARC, The properties of the ARC were measured as n = 2.16, k.= 0.88, and d = 254 A. The test wafers were then spin-coated with 10 varying thicknesses (0.554).7 pro) of undyed APEX E resist to simulate resist thickness variations such as those over device topography. ***DUV*** patterning was performed with 0.35- and 0.3-mum nominal CD lines, and linewidth vs. resist thickness was measured. Nine point measurements within each wafer were taken on a KLA 8000 with the wafer-averaged CDs plotted vs. resist thickness. As a control group, an additional set of wafers was simultaneously processed with a traditional 250-A titanium nitride ARC.

The experimental results (Fig. 8) clearly showed the titanium nitride ARC producing a classic CD swing, measured here at 9%. No discernible CD swing could be detected with the ***dielectric*** ARC, with the 3% linewidth change appearing to result primarily from resist bulk effects and measurement scatter. Although the measured linewidths tended to be slightly larger than the targeted linewidths (0.32 vs. 0.3 mum), this can be attributed to an exposure dose setting that is not optimized for the ARC film. The 9 point within-wafer measurements showed the CD uniformities to be less than 2% for all wafers. The CD swing and uniformity data confirm that PECVD-deposited ARC films meet the control requirements of an ultra-high performance ARC.

Resist profiles were examined to determine the extent of footing caused from ***DUV*** photoresist interface contamination. The traditional TiN ARC has a large footing problem; the ***dielectric*** ARC film has no footing or ***DUV*** resist contamination (Fig. 9).

Conclusion

PECVD-deposited ***dielectric*** ARC testing demonstrates its application in critical photolithography. The design of these ARC layers is facilitated by photolithography simulators. The required level of process control is within the manufacturing capabilities of single-wafer architecture deposition chambers. By following the three outlined steps (simulation, process targeting, and ***lithography*** testing), the design of similar ARCs is readily available to semiconductor manufacturers for numerous applications.

DIAGRAM: Figure 1. Resolution breakdown mechanisms from substrate reflections.

DIAGRAM: Figure 2. Phase-shift cancellation by optimization of a bottom ***dielectric*** ARC.

DIAGRAM: Figure 3. Demonstration of resist loss during pattern transfer to ARC layers: a) organic spin-on ARC; and b) ***dielectric*** ARC.

GRAPH: Figure 4. Contour map of 0%, 1%, and 3% substrate reflectivities for 220-, 240-, and 265-A ARC films. ARC film requirements are for 248-nm aluminum.

DIAGRAM: Figure 5. Refractive index of various materials at 248 nm [7].

GRAPH: Figure 6. Overlapping plots of n and k process trends and 0%, 1%, and 3% substrate reflectivity contours for 220-, 240-, and 265-A ARC films. intersection points along the zero reflectivity line represent an optimized bottom ARC. ARC film requirements are for aluminum at 248 nm. The recipes at the points of intersection between the process trends and the contour line of zero substrate reflectivity should yield the highest performing ***dielectric*** ARCs.

GRAPH: Figure 7. Simulated CD swing curves for ***dielectric*** ARC films of 0, 1, and 3% substrate reflectivity. Since the model predicts that just 1% reflectivity results in 17%-CD variation, control of the ARC process is critical.

GRAPH: Figure 8. Measured CD swing curves for ***dielectric*** ARC films and TiN using APEX E photoresist at ***DUV*** wavelength. The ***dielectric*** ARC has superior performance at both 0.35- and 0.3-mu linewidths.

DIAGRAM: Figure 9. Photoresist profiles showing that a) traditional TiN ARC can cause footing with chemically amplified ***DUV*** resists, whereas b) the ***dielectric*** ARC has no footing or resist contamination.

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Source: Solid State Technology, Mar97, Vol. 40 Issue 3, p109, 4p
Item: 9704025755

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